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An Improved Power Gating Technique for Low Power Circuits Using Asynchronous Logic

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ABSTRACT

Power consumption has become a significant concern in the design of digital integrated circuits. It is necessary to provide low power and high performance system. An improved fine grained power gating technique is presented in this paper. This work mainly focused on obtaining low power by implementing asynchronous logic. Asynchronous system design in recent years has reemerged as an important vehicle in the field of high performance, low power and secure computing. It represents an important design methodology in recent deep sub-micron technologies. High leakage current in deep-sub micrometer regimes is becoming a significant contributor to power dissipation as threshold voltage, channel length, and gate oxide thickness are reduced. Power gating is one of the most effective techniques for leakage reduction. In the proposed work, each pipeline stage in the circuit is comprised of logic gates, which implements the logic function and a handshake controller. The power to the logic blocks are controlled and supplied by the handshaking controllers. The work measures and compares the power consumption, area and delay of a 4 bit traditional Array multiplier with the proposed power gated Array multiplier using DSCH tool.

Keywords:-Asynchronous logic, power gating, low power.

INTRODUCTION

The evolution of portable or mobile communication devices such as laptops, cellular phones, video games, etc. is the most important factor driving the need for low power design.Most of the digital integrated circuits designed and fabricated today are synchronous in nature. In synchronous circuits, all components share a common time, defined by a clock signal distributed throughout the circuit. In high-speed circuits, as the clock frequency increases, power consumption also increases gradually. In modern integrated circuits, one way to reduce power consumption is to turn of power to parts of the circuit when those are idle. This method is called power gating.

Static dissipation results from leakage current. As threshold voltage, channel length, and gate oxide thickness continue to shrink, leakage dissipation is becoming a significant contributor to the total power dissipation. In a nanometer CMOS circuit, leakage power can constitute as much as a third of total power. At the circuit level, leakage reduction techniques include transistor stacking, reverse body biasing, dual threshold CMOS, and power gating. Among these techniques, power gating is one of the most effective techniques for leakage reduction. Power gating is one of the most effective techniques for leakage reduction. Power-gating is a technique for saving leakage power by shutting off the idle blocks. Asynchronous circuits employ local handshaking for transferring data between neighboring modules, so they are data-driven and active, only when performing useful work. That is, asynchronous circuits do not switch when inactive and inherently have the advantage of offering the equivalent of fine-grain clock gating.

ASYNCHRONOUS LOGIC

An effective method for reducing power consumption is reducing the dependency on the clock signal in the circuit. To achieve this, the digital system should be divided into smaller autonomous blocks. These blocks should not share a common time defined by a clock signal. This leads to the asynchronous design style. Asynchronous circuits have the advantage of going into an idle state by nature, and there will be no transitions in the circuit during the idle state. Thus, by going in for asynchronous logic, power is employed only for useful work.

Asynchronous circuits have the advantage of going into an idle state by nature, and there will be no transitions in the circuit during the idle state. Thus, by going in for asynchronous logic, power is employed only for useful work. Another favorable circumstance that influences asynchronous design is that, even in an active system, only the subsystem required for computation will dissipate power.

HANDSHAKE CONTROL

Asynchronous circuits communicate via handshakes. A handshake consists of a series of signal events sent back and forth between the communicating elements. We can divide the communicating elements into a sender and a receiver part.

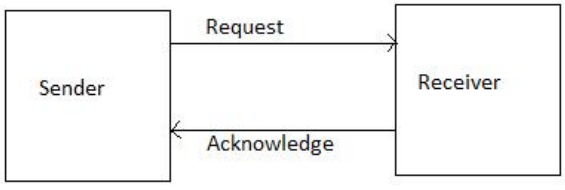

Fig.1 Sender Receiver Handshake

The sender is the element that initiates the handshake sequence. If the sender wants the receiver to perform a certain task, it makes a request to the receiver. When the receiver has finished executing the task it makes an acknowledge signal to the sender that the task has been completed. This is the way sequencing of actions is handled in asynchronous circuits by handshake communications.

PROPOSED POWER GATING TECHNIQUE

In general, power gating techniques increase the effective resistance of leakage paths.In Fine-Grain power gating approach each logic block has its own controller. The proposed power gating technique is shown in the figure 2.

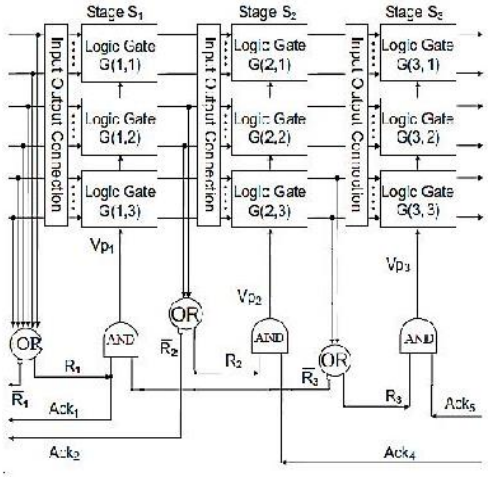

Fig.2 Proposed power gating technique

In the proposed method the given circuit is divided into a number of stages. Each pipeline stage in the circuit is comprised of logic gates, which implement the logic function of the stage, and a handshake controller, which handles handshaking with the neighboring stages and provides power to the logic gates. All the logic gates in the same pipeline stage can share a common handshake controller.

Each handshake controller consists of the following

- n input OR gate
- AND gate
- Request and Acknowledge signals

The power supply of all the logic blocks are controlled and supplied by the handshake controllers. All the inputs of a particular stage is given to the OR gate. The output of OR gate is taken as request signal. It is given as one input to the two input AND gate. The invert of alternative stage request signal is the acknowledge signal. For the first stage AND gate the second input is the third stage acknowledge signal. The output of AND gate is given as the power supply input of the stage.

In each pipeline stage, the handshake controller HCi in stage Si performs the following tasks:

1) Detecting the validity of the inputs to the logic gates in stage Si;
2) Offering power to the logic gates in stage Si ;
3) Detecting whether the outputs of stage Si have been received by the downstream stage Si+2; and
4) Informing the upstream stage Si−2 when Si−2 can remove its outputs.

The OR gate in the first handshake controller checks the validity of all inputs to the logic gates in stage S1. When at least anyone of the input is high, the OR gate sets the request signal R1 to HIGH. When both request and acknowledge signal is high the AND gate provides power supply to all the logic gates in the particular stage. Furthermore, the output of the AND gate in the handshake controller HCi is connected to the power nodes of all logic gates in stage Si , and thus all logic gates in the same stage can begin evaluating/discharging at the same time.

Thus the logic gates acquire power and become active only when performing useful computations and idle gates are not powered and thus have negligible leakage power dissipation.

LOGIC IMPLEMENTATION

The proposed power gating method is tested for a 4 bit Array multiplier. It is compared with the traditional Array multiplier. The multiplier is designed for 4 bit multiplication using DSCH tool and the corresponding layouts are obtained using Microwind 3.5 tool using 45nm technology.

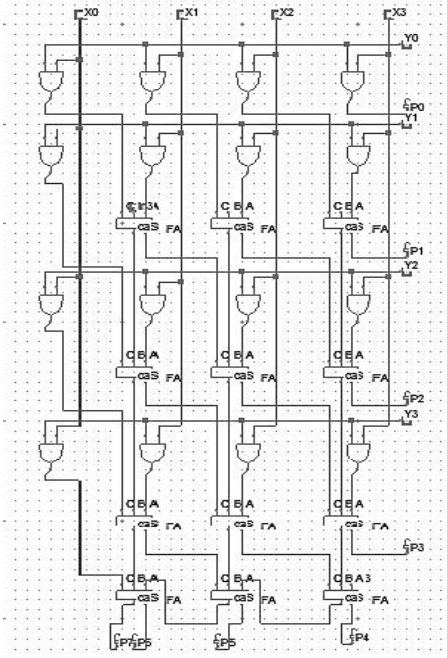

Fig.3 Schematic of the 4 bit array multiplier using DSCH 3.5 tool

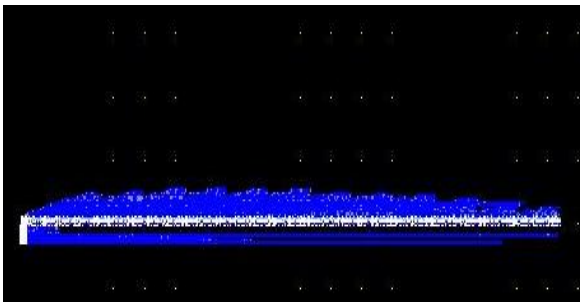

Fig.4 Layout of 4 bit array multiplier using 45nm technology

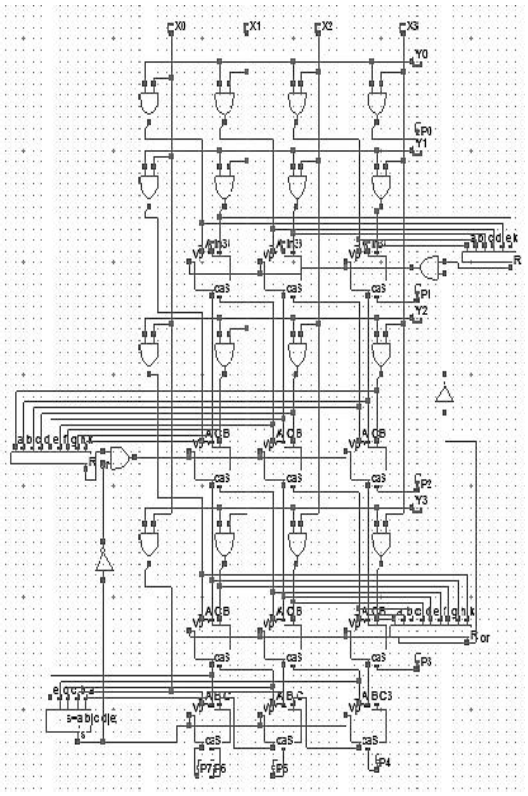

Fig.5 Schematic of the 4 bit array multiplier with power gating technique using DSCH 3.5 tool

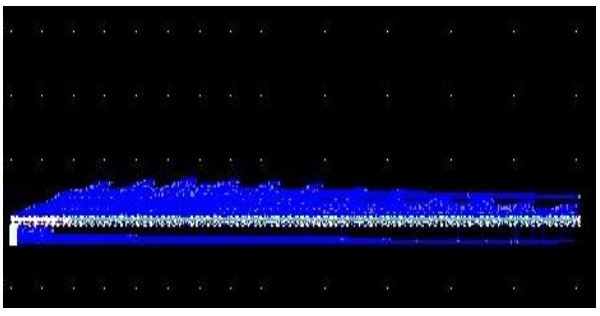

Fig.6 Layout of 4 bit array multiplier with power gating using 45nm technology

PERFORMANCE COMPARISON

The 4bit Array multiplier is synthesized and simulated using Microwind 3.5 tool using 45nm technology.

Array multiplier	Delay (ns)	Number of Transistors	Power (mw)
w/o power gating	0.249	216	2.001
With power gating	0.635	267	1.705

Table.1 Comparison of Array multiplier architectures with and without power gating

Table 1 shows the transistor count, power consumption and delay comparisons for 4 bit Array multiplier with and without power gating technique.Synthesis and analysis shows that the Array multiplier with the proposed power gating technique exhibits greater power reduction compared to the normal Array multiplier. Number of transistors and delay has been slightly increased. The reason is the need of extra controlling gates.

CONCLUSION

In this work, an improved power gating technique for low power circuits is proposed. The layout level analysis of 4 bit Array multiplier using 45nm technology shows that the proposed power gating is the most efficient in terms of power reduction. Here the logic blocks become active only when performing useful computations, and the idle logic blocks were not powered and have negligible leakage power dissipation. When the number of stages is more the proposed technique will achieve greater power reduction.

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